Code No.: 20[illegible]A2

MR12

MALLA REDDY ENGINEERING COLLEGE (AUTONOMOUS)

(Affiliated to JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD)

Gundlapochampally (H), Maisammaguda (V), Medchal (M), Medchal-Malkajgiri (Dist), Hyderabad

IV B.TECH I SEMESTER SUPPLEMENTARY EXAMINATIONS, DECEMBER-2018

Subject: **Digital Image Processing**

Branch: **ECE**

Time: 3 hours **Max. Marks: 75**

Answer any **FIVE** Questions of the following **5x15M=75M**

1. a) Write a short notes on (8M)
   i) Neighbors of pixels ii) Sampling and quantization of an image.
   b) Differentiate between Walsh and Hadamard transform. (7M)
2. a) Explain various image enhancement techniques by point processing. (8M)
   b) With the help of necessary expressions explain how differentiation is helpful in image sharpening. (7M)
3. a) Explain smoothing techniques in frequency domain for image enhancement. (8M)
   b) Explain the following techniques. (7M)
   i) Unsharp masking ii) High boost filtering
4. a) Write a short notes on Inverse filtering and Least mean square filtering. (7M)
   b) What is Wiener filter? Explain. (8M)
5. a) What is an image edge? Explain about Prewitt and Sobel operators in edge detection. (8M)
   b) Explain about Global processing via Graph-Theoretical techniques. (7M)
6. a) Draw the block diagram of image compression model and explain each block. (7M)
   b) Explain about JPEG 2000 standards. (8M)
7. a) Explain the role of wavelet transforms in image processing with examples. (7M)
   b) Write a short notes on discrete wavelet transforms. (8M)
8. a) Explain about opening and closing operations. (8M)
   b) What are logical operations involved in binary images. (7M)

Code No.: 20423

MR11/ MR12

MALLA REDDY ENGINEERING COLLEGE (AUTONOMOUS)

(Affiliated to JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD)

Gundlapochampally (H), Maisammaguda (V), Medchal (M), Medchal-Malkajgiri (Dist), Hyderabad

IV B.TECH I SEMESTER SUPPLEMENTARY EXAMINATIONS, NOVEMBER-2018

Subject: **VLSI DESIGN**

Branch: **ECE**

Time: 3 hours **Max. Marks: 75**

Answer any **FIVE** Questions of the following **5x15M=75M**

1. a) Explain the various steps involved in the N-well CMOS fabrication process with the help of neat diagrams. [10]

   b) Why ion-implantation is preferred over diffusion for impurity doping? Explain briefly ion-implantation technique. [5]

2. a) Explain about the BiCMOS inverters with neat diagrams. [7]

   b) Derive the drain current and drain voltage relationship for an N-channel Enhancement MOSFET for different regions of operation. [8]

3. a) Design a stick diagram of 'OR' gate?

   b) Design a layout for equation $Y=A\bar{B} + \bar{A}B$

4. a) Explain domino logic in detail. [8M]

   b) Compute the ON resistance (VDD to GND) of an NMOS inverter having pull-up to pull-down ratio of 4:1, if n-channel sheet resistance, Rsn = 10^4 Ω per square. [7M]

5. a) Design and explain a Manchester carry chain?

   b) Explain the SRAM with a differential pair sense amplifier?

6. a) Implement the following Boolean functions using PLA. [8]

   $F1(A,B,C) = \Sigma(1,2,4,6)$ $F2(A,B,C)=\Sigma(0,1,6,7)$ $F3(A,B,C)= \Sigma(2,4,5,6,7)$

   b) Draw and explain architecture of CPLD with neat sketches. [7]

7. a) Explain the Implementation of VHDL programming on devices using flow?

   b) Explain the RTL synthesis varied with the targeted to the Device synthesis

8. . a) What is the need of Test and Testability in VLSI system design. Explain. [8]

   b) Explain the Boundary scan system level test technique. [7]